## REMARKS

These remarks are in response to the to the Official Action mailed on July 12, 2000, requiring the Applicant to specifically apply each limitation of element of the copied claims to the disclosure of the application. This is supplied for claims 35, 36, and 38-40 below as part of the Request for Declaration of Interference, claims 37 and 41-44 having been cancelled to better focus this request.

## REQUEST FOR DECLARATION OF INTERFERENCE

It is respectfully requested that an interference be declared between the present application and patent 5,652,720 of Aulas et al., referred to below as the "`720 patent". Claims 35, 36, and 40 of the present application are exact copies of claims 37, 38 and 43, respectively, of the `720 patent. Pending claims 38 and 39 are modified versions of respective patent claims 41 and 42. Claim 35 of the present applications an exact copy of claim 37 of the `720 patent and is suggested as the count for the interference, as follows:

Count 1

A memory device comprising:

a plurality of memory cells, each of which is readable by application of a read voltage; and

means for determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results.

35 U.S.C. 135(b)

Claims 35-44 of the present application was added by Preliminary Amendment filed July 17, 1998. This is less than one year after the `720 patent was granted on July 29, 1997.

Effective Filing Date

As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by the Continuation Application Transmittal filed of August 7, 1997, the present application is entitled to an effective filing date of May 20, 1992, due to the benefit of:

U.S. Ser. No. 08/406,677, filed March 20, 1995, now patent no. 5,657,332,

U.S. Ser. No. 07/886,030, filed May 20, 1992.

The `720 patent is shown to have a United States filing date of December 18, 1995, claiming priority from a French application of December 20, 1994. Thus, the earliest priority date noted on the `720 patent is over two years later than the May 20, 1992, effective filing date of the present application.

Therefore, it is requested that the interference be declared with the Applicants of the present application designated the senior party.

Claims Corresponding to the Proposed Count 1

The proposed count 1 is an exact copy of claim 37 of the `720 patent. Claims 41-43 of the `720 patent are all dependent upon claim 37 and provide more detail for the two elements of this base claim. Claim 38 also depends on claim 37 and provides an additional element for the rewriting of data.

Support for the Proposed Count 1 in the Present Application

| Count 1 | Present Application |
|---|---|
| A memory device comprising: | All of the described embodiments are memory devices. |
| a plurality of memory cells, each of which is readable by application of a read voltage; and | Figure 1b shows a memory cell and Figures 2a and 2b arrangements of a plurality of such cells as described beginning at page 11, line 32. |

Reading a cell by the application of a voltage is described with respect to the exemplary values of Figure 3 on page 13 at line 10.

means for determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results.

This is shown in Figure 4 as READ CIRCUIT 213, the determining illustrated with respect to Figures 6a and 6b beginning at page 18, line 18: "a memory cell 601 whose control gate is connected to a multiplexor ... [which] receives at its inputs the several voltage sources". (p. 18, lns. 20-24) The first terminal is the control gate and various of the voltages and their relation and exemplary values are given in Figures 10 and 11. The determining a likelihood that the memory device is degraded are steps 805 using $V_{PRH}$ and 807 using $V_{PRI}$ for the programming algorithm of Figure 8, or are steps 902 using $V_{SH}$ and 904 using $V_{SL}$ for the scrubbing algorithm. These algorithm are described beginning, respectively, at page 23, line 6, and at page 24, line 27.

Support for Pending Claims 36 and 38-40 Present Application

| Claim 36 | Present Application |
| --- | --- |
| The memory device of claim 35, wherein a group of the plurality of memory cells are arranged in a row that includes the cell, the memory device further comprising means for rewriting a previously stored value into each of the group of memory cells when the means for determining determines that the first cell has a degraded state. | For claim 35, see above. Figure 2a shows the cells arranged into rows, the group of the cell part of a row in the "Second Sector" of the scrub algorithm of Figure 9. The writing means is PROGRAM CIRCUIT of Figure 4. The cell is determined to be in a degraded state in the "NO" path from both step 902 and 904, the rewriting being step 905. |

| Claim 38 | Present Application |
| --- | --- |
| The memory device of claim 35, wherein: | For claim 35, see above. |
| a group of the plurality of memory cells are arranged in a row that includes the first cell; and | Figure 2a shows the cells arranged into rows, the group of the cell part of a row in the sectors being programmed in the algorithm of Figure 8. |
| the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a write is performed on the group of memory cells. | Figure 8 is the algorithm for writing date into the group of memory cells at step 801. Applying each of the plurality of read voltages during a write corresponds to steps 803 and 805 of Figure 8, or alternately, as part of the scrub of step 808, during steps 902 and 904 of the scrub algorithm of Figure 9. |

| Claim 39 | Present Application |
| --- | --- |
| The memory device of claim 35, wherein: | For claim 35, see above. |
| a group of the plurality of memory cells are arranged in a row that includes the first cell; and | Figure 2a shows the cells arranged into rows, the group of the cell being part of a row in the sector being read. |
| the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a read is performed on the group of memory cells. | "Additionally, a scrub during read implementation of the present invention, analogous to the scrub during write provides still further reliability improvements." (p. 25, lns. 27-30) |

| Claim 40 | Present Application |
| --- | --- |
| The memory device of claim 35, wherein the terminal of the first cell is a control gate terminal of the first cell. | This has already be given above with respect to claim 35: "a memory cell 601 whose control gate is connected to a multiplexor ... [which] receives at its inputs the several voltage sources". (p. 18, lns. 20-24) |

`720 Patent Prosecution File History

A review of the file history of the `720 patent reveals that the material in the present application was not cited during the `720 patent application process.

Conclusion

A prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application or disclosure statements, a telephone call to the undersigned is invited.

Dated:

Respectfully submitted,

By: _____

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Atty. Docket: HARI.026US3